What is claimed is:

1. An insert for seating an electronic device comprising a chip-scale package having electrical-contact bumps and a protrusion prjecting from a common side thereof, said insert comprising:

   a substrate having walls defining a plurality of pockets configured to receive at least a portion of the electrical-contact bumps of said chip-scale-package, other walls of said substrate defining a clearance recess configured to receive with clearance the protrusion of said chip-scale-package when the electrical contact bumps are at least partially received in said plurality of pockets; and

   conductive material within at least a portion of at least some of said plurality of pockets.

2. An insert according to claim 1, wherein said recess has a perimeter encompassing an area greater than any of said pockets.

3. An insert according to claim 2, wherein said pockets each have a width less than 400 μm and said recess has a width greater than 500 μm.

4. An insert according to claim 3, wherein said pockets each have a width between 100-400 μm, and said recess a width between 2,000-3,000 μm and length between 4,000 to 15,000 μm.

5. An insert according to claim 3, wherein said pockets and said recess have substantially the same depth.

6. An insert according to claim 5, wherein said depth is at least 10 μm.

7. An insert according to claim 3, wherein said pockets and said recess have a depth between 15-150 μm.

8. An insert according to claim 2, wherein said recess is disposed between at least two pockets of said plurality of pockets.

9. An insert according to claim 1, wherein said substrate comprises monocrystaline silicon.

10. An insert according to claim 9, further comprising a layer of dielectric material disposed conformably against said silicon of said substrate and beneath said conductive material.

11. An insert according to claim 10, wherein said dielectric material comprises an oxide.

12. An insert according to claim 10, wherein said conductive material comprises at least one of the group consisting of refractory metal, refractory metal nitride, and refractory metal salicide.

13. An insert according to claim 1, wherein said conductive material comprises at least one of the group consisting of group IIIB through VIIIB metals.

14. An insert according to claim 13, wherein said conductive material that lines said pockets is selected to resist bonding to the outwardly-projecting electrical-contact bumps of said chip-scale-package.

15. An insert according to claim 1, wherein said conductive material that lines said pockets is selected to resist bonding to solder.

16. A ball-grid-array socket for seating a microelectronic device having an array of contact-bumps and a protrusion projecting from a common side thereof, said ball-grid-array socket comprising:

a substrate with a primary surface having a plurality of pockets disposed in a pattern thereacross corresponding to said array of contact-bumps of the microelectronic device, said pockets configured to at least partially receive said contact-bumps of the microelectronic device, said primary surface of said substrate further defining a recess configured to receive and clear the protrusion of the microelectronic device when the contact bumps are at least partially received in respective said pockets of said substrate, said recess disposed amongst said plurality of pockets; and

electrically conductive material layered conformably over at least a portion of said substrate including at least some of said plurality of pockets.

17. A ball-grid-array socket according to claim 16, wherein said substrate comprises monocrystaline silicon.

18. A ball-grid-array socket according to claim 17, further comprising a layer of dielectric disposed conformably against said silicon substrate and beneath said electrically conductive material.

19. A ball-grid-array socket according to claim 18, wherein said dielectric comprises an oxide.

20. A ball-grid-array socket according to claim 17, wherein said silicon has a <100> lattice-plane of orientation at said primary surface.

21. A ball-grid-array socket according to claim 16, wherein said walls defining said pockets are sloped with an angle of about 40-70 degrees relative a plane defined by said primary surface.

22. An interconnect for electrically interfacing an electronic component, said electronic component having a protrusion and a plurality of outwardly-projecting contact-bumps extending outwardly from a front surface thereof, said interconnect comprising:

a substrate having a primary surface with a plurality of pockets configured to at least partially contact respective said outwardly-projecting contact-bumps of said electronic component, said primary surface further having a clearance recess configured to receive with clearance the protrusion of the electronic component when said contact-bumps are at least partially contacting associated said plurality of pockets; and

conductive material patterned over at least a portion of the primary surface of said substrate and extending into at least one of said plurality of pockets.

23. An interconnect according to claim 22, wherein said pockets associated with respective said outwardly-projecting contact-bumps each have a first width, said protrusion has a second width greater than said first width, and said clearance recess has a width greater than said second width for enabling clearance of said protrusion.

24. An interconnect according to claim 23, wherein said clearance recess has a depth of at least 10 μm.

25. An interconnect according to claim 24, wherein said substrate comprises silicon.

26. An interconnect according to claim 25, wherein said silicon has a <100> plane of orientation at said primary surface.

27. An interconnect according to claim 25, wherein said substrate has a thickness of at least 500 μm.

28. An interposer for interfacing an electronic component having a protrusion and a plurality of contact-bumps that extend outwardly from a front face thereof, said interposer comprising:

a substrate having a primary surface with a plurality of pockets disposed thereacross, said plurality of pockets configured to at least partially receive respective said plurality of contact-bumps of said electronic component, said primary surface further comprising a recess configured to receive with clearance the protrusion of the electronic component when said contact-bumps are at least partially received within associated said plurality of pockets;

conductive material patterned over the primary surface of said substrate including at least one of said plurality of pockets; and

an electrical terminal disposed on said substrate and electrically coupled to said at least one pocket by a portion of said patterned conductive material.

29. An interposer according to claim 28, wherein said substrate comprises silicon.

30. An interposer according to claim 29, wherein said silicon has a <100> lattice plane of orientation at said primary surface.

31. An interposer according to claim 30, wherein said walls that define said pockets have a slope of about 40-70° relative said primary surface.

32. An interposer according to claim 31, wherein said one pocket that receives said protrusion has a depth of at least 10 μm.

33. An interposer according to claim 32, further comprising a dielectric layer conformably layered over said substrate and beneath said patterned conductive material.

34. An interposer according to claim 33, wherein said dielectric comprises oxide.

35. An interposer according to claim 33, wherein said substrate has an outer peripheral edge and said electrical terminal is disposed proximate said outer peripheral edge.

36. A method of interfacing an electronic device comprising the steps of:

providing an electronic device having a plurality of contact-bumps of a ball-grid-array and an encapsulant projection that extend outwardly from a face thereof;

providing a substrate having a primary surface with a plurality of pockets disposed thereacross corresponding to said plurality of contact-bumps of the ball-grid-array of said electronic device, said primary surface further comrising a recess;

disposing said electronic device over said substrate;

contacting at least part of each of said contact-bumps of said electronic device with respective said plurality of pockets of said substrate; and

receiving and clearing said encapsulant projection of said electronic device within said recess of said substrate.

37. A method according to claim 36, further comprising a step of propagating an electrical signal between said substrate and said electronic device.

38. A method according to claim 37, wherein said step of propogating includes transferring said electrical signal between a contact-bump of the electronic device and the respective pocket of said plurality engaged therewith.

39. A method of testing an electronic device comprising steps of:

providing a chip-scale-packaged electronic device, said chip-scale-package having a protrusion and a plurality of outwardly-projecting contact-bumps that extend outwardly from a face thereof;

providing a substrate having walls that define a plurality of pockets across a surface thereof, at least one of said plurality of pockets configured to at least partially receive respective one of said plurality of contact-bumps of the chip-scale-package, other walls of said substrate defining a recess configured to receive the protrusion of the electronic device;

coupling said electronic device to said substrate with said at least one contact bumps at least partially contacting associated said plurality of pockets and said protrusion positioned within said recess without contacting the walls defining said recess; and

propagating at least one electrical signal between said substrate and said electronic device.

40. A method according to claim 39, further comprising a step of removing said electronic device from said substrate after propagating the electrical signal.

41. A method according to claim 39, wherein an electrical signal is propagated between a contact-bump of the electronic device and a pocket of said substrate.

42. A method of fabricating an insert for interfacing an electronic device having a plurality of contact-bumps and a protrusion that extend outwardly from a face thereof, said method comprising the steps of:

providing a substrate;

forming a plurality of pockets in said substrate;

forming a recess in said substrate having a width and length, the width and length of said recess being greater than the respective widths of any of said pockets;

forming a layer of insulating material conformably over said substrate, including said plurality of pockets; and

forming conductive material over said insulating material, including at least a portion of said pockets.

43. A method according to claim 42, wherein said plurality of pockets and said recess are formed in a single step of etching.

44. A method according to claim 43, wherein said step of etching comprises an anisotropic wet etch.

45. A method according to claim 44, wherein said substrate comprises monocrystalline silicon with a <100> surface plane.

46. A method according to claim 43, wherein said pockets and said recess are formed with a depth of at least 10 μm.

47. A method according to claim 46, wherein said pockets and said recess are formed with a depth of about 15-150 μm.

48. A method according to claim 42, wherein said step of forming the conductive material over said substrate comprises the steps of:

layering metal conformably over said substrate; and

clearing portions of said metal from regions of said substrate corresponding to said recess.

49. A method of fabricating a ball-grid-array socket for an electronic device comprising a chip-scale-package having an array of outwardly-projecting contact-bumps and an encapsulant-projection, said method comprising the steps of:

providing a substrate;

etching said substrate and forming a trench in said substrate and an array of pits in said substrate disposed on at least two opposite sides of said trench, said array of pits formed to at least partially contact respective said outwardly-projecting contact bumps of said chip-scale-packaged electronic device and said trench formed with a length and a width greater than that of any pit of said plurality to enable receipt with clearance of the encapsulant-protrusion of said chip-scale-packaged electronic device;

forming an insulating layer conformably over said substrate, incuding said pits;

forming conductive material in at least some of said pits; and

forming a conductive trace on the substrate in electrical communication with the conductive material of at least one of said pits.

50. A method according to claim 49, wherein said step of etching comprises an anisotropic wet etch.

51. A method according to claim 50, wherein said substrate comprises monocrystalline silicon having a <100> surface plane.

52. A method according to claim 49, wherein said pit and trench are formed with a depth of at least 10 μm.

53. A method according to claim 52, wherein said pit and trench are formed with a depth in the range of 15-150 μm.

54. A method according to claim 49, further comprising a step of forming a via in said substrate.

55. A method according to claim 54, wherein said via is formed in communication with a pit of said array of pits.

56. A method according to claim 54, wherein said via is formed between a floor of a pit of said array of pits and a surface of said substrate opposite said array of pits.

57. A method according to claim 54, wherein said step of forming the via employs a laser beam.

58. A method according to claim 54, wherein said via is formed with walls substantially perpendicular to a surface of said substrate.

59. A method according to claim 58, wherein sidewalls of said array of pits are formed with a slope between 40-70° relative said surface of said substrate.

60. A method according to claim 54, wherein said step of forming the insulating layer includes coating sidewalls of said via with insulating material.

61. A method according to claim 60, wherein said step of forming the insulating layer comprises a step of exposing said substrate to an oxidizing environment.

62. A method according to claim 54, further comprising a step of forming conductive material within said via.

63. A method according to claim 62, wherein said step of forming conductive material within said via employs chemical-vapor-deposition.

64. A method according to claim 62, wherein said step of lining electrically couples a pit to conductive material in said via.

65. A method according to claim 62, wherein said step of forming conductive material in at least some of said pits comprises a step of depositing conductive material different from that within said via.

66. A method according to claim 54, further comprising a step of fixing a contact bump to an exposed surface of the conductive material in the via on a side of said substrate opposite said pocket.

67. A method according to claim 66, wherein said contact bump comprises a solder bump.

68. A method according to claim 67, wherein said contact bump comprises a tin/lead eutectic.

69. An insert for interfacing an electronic device having a plurality of outwardly-projecting-contacts, said insert comprising:

a substrate, walls of said substrate defining at least one pocket configured to receive an outwardly-projecting contact of the electronic device, other walls of said substrate defining a via through said substrate;

conductive material disposed in said via; and

second conductive material disposed in said at least one pocket, and over the conductive material in said via.

70. An insert according to claim 69, wherein said substrate comprises monocrystaline silicon.

71. An insert according to claim 69, wherein opposing walls that define said pocket are inclined with an angle of about 40-70 degrees relative a plane defined by a surface of said substrate.

72. An insert according to claim 69, wherein the walls defining said via adjoin a floor of said pocket.

73. An insert according to claim 69, further comprising dielectric between said conductive materials and said substrate.

74. An insert according to claim 69, further comprising an electrical-contact-bump disposed upon said substrate and over the region defined by where said via meets a surface of said substrate opposite said pocket.

75. An insert according to claim 74, wherein said electrical-contact-bump comprises solder.

76. A BGA test socket for temporarily engaging a plurality of outwardly-projecting contacts of a BGA of a microelectronic device, said test socket comprising:

a substrate, first walls of said substrate defining a pocket configured to seat an outwardly-projecting contact of the microelectronic device, and second walls of said substrate defining a passage through said substrate in communication with said pocket;

first conductive material within at least a portion of said passage; and

second conductive material conformably layered in at least a portion of said pocket and over said first conductive material.

77. A BGA test socket according to claim 76, wherein said substrate comprises silicon having a <100> lattice-plane of orientation at an outwardly facing surface thereof.

78. A BGA test socket according to claim 76, wherein sidewalls of said walls that define said pocket are sloped about 40-70 degrees relative a surface of said substrate.

79. A BGA test socket according to claim 76, wherein the walls defining said passage meet a wall of said walls defining said pocket.

80. A BGA test socket according to claim 76, further comprising a layer of insulating material between said first and said second conductive materials and said substrate.

81. A BGA test socket according to claim 76, wherein the walls of said passage meet a lower surface of said substrate to define an aperature and said BGA test socket further comprises a contact-bump fixed to said substrate over said aperature and electrically coupled to the first conductive material within said passage.

82. A BGA test socket according to claim 81, wherein said contact-bump comprises reflowable conductive material.

83. A BGA test socket according to claim 82, wherin said contact-bump comprises a tin/lead alloy.

84. A BGA test socket according to claim 82, further comprising a support substate having a conductive contact pad, said substrate fixed to said support substrate with said contact-bump joined to said conductive contact pad.

85. A BGA test socket according to claim 84, wherein said substrate comprises mono-crystaline silicon and said support substrate comprises dielectric material.

86. A method of forming a BGA socket for testing a microelectronic device comprisin a chip-scale-package having a plurality of outwardly-projecting-contacts, said method comprising steps of:

providing a substrate;

forming a pocket in said substrate configured to at least partially receive an outwardly-projecting-contact of said chip-scale- packaged microelectronic device;

forming a via through said substrate;

forming first electrically conductive material in said via; and

depositing second electrically conductive material in at least a portion of said pocket, including a portion over the first electrically conductive material in said via.

87. A method according to claim 86, wherein said step of forming said pocket comprises forming sidewalls for said pocket that are sloped about 40-70° relative a surface of said substrate.

88. A method according to claim 86, wherein said substrate comprises monocrystaline silicon having a <100> lattice-plane of orientation at a surface thereof.

89. A method according to claim 86, further comprising a step of forming an insulating layer over said substrate including said pocket and said via.

90. A method according to claim 89, wherein said step of forming an insulating layer comprises a step of exposing said substrate to an oxidizing atmosphere.

91. A method according to claim 86, wherein said step of forming first conductive material in said via comprises a step of chemical-vapor-deposition.

92. A method according to claim 86, wherein said second electrically conductive material is different from said first electrically conductive material.

93. A method according to claim 86, further comprising a step of fixing said substrate to a support substrate with said pocket facing away from said support substrate.

94. A method according to claim 86, further comprising a step of forming a conductive-contact on a side of said substrate opposite said pocket, said conductive-contact coupled to a portion of said first electrically conductive material in said via.

95. A method according to claim 94, further comprising the steps of:

providing a support substrate having a conductive-pad; and

joining the conductive-contact of said substrate to the conductive-pad of said support substrate.

96. A method according to claim 95, wherein the conductive-contact of said substrate comprises a flowable metal alloy and the conductive-pad of said support substrate comprises conductive material wetable by said flowable metal alloy, and said step of fixing said substrate to the support substrate comprises the steps of:

positioning the conductive-contact of said substrate in contact with the conductive-pad of said support substrate;

heating and re-flowing the flowable metal alloy of the conductive-contact; and

wetting the conductive-pad of said support substrate with the heated re-flow of said flowable metal alloy.

97. A method according to claim 96, wherein the first conductive material is selected to be wetable by reflow of the flowable metal alloy of said conductive-contact.

98. A method according to claim 97, wherein the second conductive material is different from said first electrically conductive material.

99. A method according to claim 98, wherein the second electrically conductive material is selected to resist bonding to the outwardly-projecting-contacts of a chip-scale-packaged microelectronic device.

100. A method according to claim 98, wherein the second electrically conductive material is selected to resist bonding to solder.

101. A method according to claim 86, wherein walls defining said via are formed substantially perpendicular to an upper surface of said substrate and sidewalls of said pocket are sloped with an angle between 40-70° relative to said upper surface.

102. A method according to claim 101, wherein the walls defining said via join a floor of said pocket.

103. A method of testing a microelectronic device, said method comprising:

providing a microelectronic device having a plurality of outwardly-projecting-contacts of a BGA;

providing a test insert comprising

a silicon substrate having walls that define a plurality of pockets configured to at least partially receive respective said plurality of outwardly-projecting-contacts, other walls of said silicon substrate defining a via extending through said silicon substrate,

first conductive material in said via and at least a portion of at least one of said pockets, and

a conductive-contact on a side of said silicon substrate opposite said pocket and electrically coupled to said pocket by way of said via;

fixing said test insert to a support substrate with the conductive-contact of said test insert coupled to a conductive-pad of said support substrate;

disposing said microelectronic device over said test insert with the plurality of pockets of said test insert removably coupled to respective ones of said plurality of outwardly-projecting-contacts of the microelectronic device; and

propogating an electrical signal between said support substrate and said microelectronic device by way of said test insert.

104. A method according to claim 103, wherein the conductive-contact of said test insert comprises a flowable metal alloy and the conductive-pad of said support substrate comprises conductive material wetable by said flowable metal alloy, and said step of fixing said test insert to the support substrate comprises the steps of:

positioning the conductive-contact of said test insert in contact with the conductive-pad of said support substrate,

heating and re-flowing the flowable metal alloy of said conductive-contact, and

wetting the conductive-pad of said support substrate with the re-flow of said flowable metal alloy.

105. A method according to claim 104, wherein the conductive-contact of said test insert comprises a solder bump.

106. A method according to claim 103, further comprising a step of forceably biasing said microelectronic device against said test insert to facilitate electrical coupling of the plurality of pockets of said test insert with respective ones of said plurality of outwardly-projecting-contacts of the microelectronic device.